Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS

1. (*Previously Presented*) A power semiconductor device comprising:

a semiconductor substrate with two surfaces, an N+ doped layer extending into the substrate from one surface thereof, an N- doped layer over the N+ doped layer, a P-doped well formed in the N- doped layer and extending from the other surface of the substrate into the N- doped layer, a P+ doped region formed in the P- doped well and extending from the other surface of the substrate into the P-doped well, an N+ doped region formed in the other surface of the substrate and in the N- doped layer, said N+ region laterally spaced from the P+ doped region and the P-doped well, said P- doped well and P+ doped region having a combined thickness of about 5μm to about 12 μm; and

recombination centers comprising noble metal impurities disposed substantially in said N - doped layer and P - doped well.

2. (*Previously Presented*) The device of claim 1 wherein said P - doped well has a thickness of about 4 μm to about 10 μm.

3. (*Previously Presented*) The device of claim 1 wherein said P+ doped region has a thickness of about 0.1 μm to about 2 μm.

4. (*Previously Presented*) The device of claim 1 wherein said P - doped well has a dopant level of at least 10^{16} atoms/cm^3.

5. (*Previously Presented*) The device of claim 4 wherein said P - doped well has a dopant level of about 2.5x 10^{17} atoms/cm^3.

6. (*Previously Presented*) The device of claim 1 wherein said P+ doped region has a dopant level of at least 10^{18} atoms/cm^3.

7. (*Previously Presented*) The device of claim 6 wherein said P+ doped region has a dopant level of about 6x10^{19} atoms/cm^3.

8. (*Previously Presented*) The device of claim 1 wherein said N - doped layer has a dopant level of about 10^{14} atoms/cm^3 to about 10^{15} atoms/cm^3.

9. (*Cancelled*).

10. (*Original*) The device of claim 1 wherein said noble metal impurities are selected from the group consisting of gold, platinum, and palladium.

11. (*Original*) The device of claim 10 wherein said noble metal impurities comprise platinum.

12. (*Previously Presented*) The device of claim 11 wherein said recombination centers are formed by platinum diffusion through said N + doped substrate into said N - doped and P - doped well.

13. (*Original*) The device of claim 11 containing platinum impurities at a concentration of about 1x10^{15} to about 1x10^{16} atoms/cm^3.

14. (*Original*) The device of claim 13 wherein said concentration of platinum impurities is about 2 x10^{15} atoms/cm^3.

15. (*Cancelled*).

16. (*Cancelled*).

17. (*Currently Amended*) The device of claim [[16]]1 comprising a diode, MOSFET or an IGBT power device.

18. – 34. (*Cancelled*)

35. *(Previously Presented)* A power semiconductor device comprising:

a semiconductor substrate with two surfaces, an N+ doped layer extending into the substrate from one surface thereof, an N- doped layer over the N+ doped layer, a P-doped well formed in the N- doped layer and extending from the other surface of the substrate into the N- doped layer, said P-layer having a first thickness and forming a first boundary with the N- doped layer, a P+ doped region formed in the P- doped well and extending from the other surface of the substrate into the P-doped well to have a second thickness and to form a second boundary between the P+ doped region and the P- doped well, an N+ doped region formed in the other surface of the substrate, said N+ doped region having a third thickness and forming a third boundary between the N+ doped region and the P-well or the N-doped layer,

wherein the P+ doped region is vertically thinner than the P- doped well and vertically thinner than the N+ doped region , and

recombination centers comprising noble metal impurities disposed in said N- doped layer and said P - doped well.

36. (*Currently Amended)* The device of claim 35 wherein the maximum depth of the second boundary is ~~more shallow~~ less than the first or third boundaries.

37. *(Previously Presented)* The device of claim 35 wherein the ratio of thickness of the P+ doped region to the P-doped well is between 1:40 and 1:5.

38. *(Previously Presented)* The device of claim 37 wherein the P+ doped region is between 0.1 to 2.0 μm thick and the P-doped well is between 4.0 and 10.0 μm thick.

39. *(Previously Presented)* The device of claim 35 wherein the N+ doped region is separated from the P-doped well by the N- doped layer.

40. *(Previously Presented)* The device of claim 35 wherein the N+ doped region is within the P-doped well.

41. *(Previously Presented)* The device of claim 40 wherein the N+ doped region abuts the P+ doped region.